Moscape Adds Predictability to Deep Submicron Designs With its Unique Assertion-Based Technology; ATI Research and Lara Technology Claim Significant Benefits

SAN JOSE, Calif.--(BUSINESS WIRE)--May 24, 1999--

Moscape, Inc. announced today its DesignScopes(TM) tool suite for predicting critical circuit issues related to deep submicron IC designs.

Moscape's patented assertion-based technology enables designers to uncover several implementation issues to increase quality and performance of their design prior to tapeout.

DesignScopes (Static COmprehensive Predictability Enhancement Solutions) "scopes out" potential problems such as circuit integrity, noise margins and interconnect coupling, using patented rules-based context-sensitive analysis. This increases the predictability of design with a cohesive design methodology. Starting with a built-in set of assertions and intelligence, the technology enables continuous enhancement and refinement of the rules, i.e. as new problems are encountered, the rule-set is automatically enhanced each time. Thus it provides exhaustive coverage and increasing benefit with every use.

"By building predictability into the design flow, sub-optimal design constructions, excessive design iterations and expensive silicon re-spins can be eliminated," said Chandra Somanathan, president and co-founder of Moscape. "Predictability is the real problem and it is getting worse with the increasing intricacies of DSM technologies. Predictability means going through various design phases without encountering unexpected design integrity problems that compromise performance and quality of designs."

Targeted semiconductor designs include System-On-Chip (SOC), microprocessors, media and graphics processors, communications ICs and highly integrated ASICs.

CircuitScope: Integral Part of Predictable Circuit Design Flow

CircuitScope(TM) is the first tool in the DesignScopes suite and is the first commercially available tool of its kind. This production-proven tool provides exhaustive analysis of multimillion transistor ICs, guaranteeing complete coverage of all recognized circuit structures for potential circuit integrity problems such as inconsistent circuit constructions, beta mismatch, charge-sharing, static noise margins and coupling. By performing this analysis in pre- and post-layout phases, the need for extensive back-end circuit and timing simulations is reduced while assuring greater probability of success with first silicon.

Among several customers currently using CircuitScope in production is ATI Research, Inc. (Santa Clara, Calif.), the industry's leading media processor company that developed a 12-million transistor, 500MHz, media processor using a 0.25 micron process.

"CircuitScope saved us significant design time since it was able to quickly locate many circuit problems without need for detailed SPICE simulations," said Steve Hale, circuit design manager at ATI Research. "CircuitScope also allows our design methodology to be more portable, so that parts of the chip can be designed at multiple locations with the same design correctness enforced."

Lara Technology (San Jose, Calif.) has developed a Silicon Search Engine based on content addressable memory (CAM) in a

0.18 micron process. This CAM has a search latency of 20ns, 300MHz throughput and consists of three million transistors.

"We were getting extremely productive results in just two weeks," said Eric Voelkel, director of Specialty Memory Engineering at Lara Technology. "CircuitScope analyzed a 700,000 transistor design in about an hour and we could focus on the right critical paths to fix circuit integrity issues."

There are numerous approaches for building in predictability and circuit integrity into the design flow. Some design teams use internally developed scripts and tools to spot check potentially fatal circuit conditions, but they are project specific and do not easily exploit the skills of various design experts. Circuit level simulations (e.g. SPICE), another common method, is time consuming and extraction-based analysis occurs too late in the design cycle.

"With today's traditional predictability models and methodologies, it is still very difficult to move through the design stages, from HDL to circuits to layout (GDSII) and still maintain the integrity of the design," said Nitin Deo, vice president of marketing at Moscape. "If design integrity issues are predicted at every step of the design flow, they could be fixed or avoided before becoming a problem. Ultimately, predictability analysis will become as integral to IC design as synthesis, timing analysis and layout."

Comprehensive and Fast

Operating at the transistor level, CircuitScope uses proven context-based analysis techniques to locate circuit integrity and noise problems. For a circuit structure under analysis, both driver and receiver logic contexts are analyzed. CircuitScope uncovers hazardous circuit topologies and flags circuit structures that are susceptible to coupling and crosstalk, noise sensitivity, charge-sharing, under/over-driven nodes and other critical design integrity problems.

CircuitScope classifies circuits into complementary, dynamic, ratioed and cascode logic. It then maps circuits into corresponding library components. This built-in library contains combinatorial cells, sequential cells, RAMs, tristates and several other circuit structures. CircuitScope uses the library classification to perform additional circuit integrity checking.

The tool also comes with pre-defined, customizable and open APIs that enable specification of unlimited number of user-definable assertions or rules. Users can add proprietary circuit structures or library elements along with associated checks.

CircuitScope fits into existing design flows and works with a variety of third-party tools, enabling quick migration to new processes and new projects. Industry-standard data formats such as gate-level Verilog, SPICE (hierarchical or flat) netlist, DSPF and SDF are all accepted.

Pricing and Availability

CircuitScope is currently available on Solaris, WindowsNT, HP/UX and Linux platforms. Pricing begins at $95,000 for a floating license.

For more information contact 800/635-6488 or sales@moscape.com, http://www.moscape.com.

Moscape, Inc., Santa Clara, Calif. develops and markets rules-based, static analysis tools for predicting design integrity problems in deep submicron ICs. The company was founded in 1997 and is privately held.