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Moscape spins deep-submicron analysis tool

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SAN JOSE, Calif. — Moscape Inc. will bring deep-submicron analysis further up in the IC design process this week with its first tool release, CircuitScope v2.0.

The tool, targeting structured custom design, has been maturing in the design flow at companies like Lara Technology and ATI Research over the past year. But Moscape president Chandra Somanathan said the tool is now ready for prime time.

"CircuitScope has been used with great success at leading-edge companies for leading-edge designs," said Somanathan. "We bring a unique and highly effective approach to deep-submicron analysis."

CircuitScope v2.0 is a transistor-level static analysis tool that can be used after synthesis or layout and again after place and route to detect circuit integrity, topology and noise issues. The tool flags circuits susceptible to coupling, charge, sharing, under- and overdriven nodes, electromigration and other design-integrity problems.

Nitin Deo, vice president of marketing at Moscape (Santa Clara, Calif.), said the tool brings predictability to full-custom designers who are working at process geometries of 0.25 micron and below and are encountering deep-submicron problems for the first time.

Scoping out errors

"Predictability is the real deep-submicron design challenge," said Deo. "Designers need a way to scope out unforeseen errors. Our tool allows designers to . . . find those areas where they need to concentrate their efforts."

The tool classifies circuits into complementary, dynamic, ratioed and cascode logic, the company said, then maps them into corresponding library components.

This built-in library contains combinatorial cells, sequential cells, RAMs, tristates and several other circuit structures. The tool uses the library classification to perform additional circuit-integrity checking.

It also checks "assertions" that verify circuit function. These assertions direct the tool to search for specific problems. For instance, it can ensure that regenerative nodes driving a bus don't overpower the driver; that static circuits properly drive dynamic circuits; or that a piece of logic has good noise immunity.

In "maturing" the tool at customer sites, the company built in open APIs that allow users to add their own customized assertions. The tool fits into existing flows. It accepts industry-standard formats such as gate-level Verilog, flat or hierarchical Spice net-lists, DSPF and SDF. When users find problem areas the tool can quickly generate a Spice deck for on-the-spot simulation.

The tool runs on Linux as well as Solaris, Windows NT and HP/UX platforms. Pricing starts at $95,000. The company will show CircuitScope at next month's Design Automation Conference in New Orleans.

Somanathan said Moscape is working on a gate-level version of the tool targeting ASIC designers.