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Moscaped, Inc., Pioneers Customizable Assertion Based Analysis and Repair Technology (CART(TM)) for High Performance Deep Submicron IC Designs.

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SAN JOSE, Calif., June 3 /PRNewswire/ -- EDA start-up Moscape, Inc., founded in July 1997 and headquartered in San Jose, California, announced today their proprietary and proven Customizable Assertion-based Analysis and Repair Technology (CART(TM)) aimed at improving performance and reliability of complex deep submicron IC designs. The company will be premiering their technology and products at the upcoming 35th Design Automation Conference held June 15-19 in San Francisco, CA.

The company is privately held and has raised around \$1 million from private investors including industry veterans Atiq Raza and Dr. Prabhu Goel. Company has a strong Technical Advisory Board comprised of individuals with both academic and industry repute.

Moscape has assembled a strong and experienced team and is actively expanding its infrastructure and operations. Company's principals Chandra Somanathan, Steve Parks and Dr. Rajit Chandra have combined 50+ years of extensive hands-on experience in designing several generations of complex high-performance Deep Submicron ICs such as the DEC Alpha Processors and developing state of the art EDA CAD software at companies such as Digital Equipment Corp., Intel, Bell Labs, Exponential, Cadence and Synopsys.

Moscape released a Beta version of its initial product earlier this year and has already engaged with three major reference customers in the Processors and ASIC/COT markets. Moscape's products run on Unix, Windows NT and Linux-based platforms. Company is currently targeting the ASIC/COT, Processor and IP Cores market segments.

Shrinking device feature sizes, high-frequency clocking, increased levels of design integration, significant submicron parasitics, interconnect delays and use of MixnMatch(TM) design paradigms have necessitated state of the art CAD tools to address critical performance and reliability problems in complex DSM IC designs. Moscape's technology and products deliver proven solutions to address these critical design verification needs.

Custom and standard cell-based designs that use complex static and dynamic circuits are analyzed using a unified engine working on mixed gate and transistor level representations. It statically analyzes and repairs circuit failure conditions in the pre- and post-layout phases of a design.

Moscape's products tightly integrate logic and physical design domains and enable significant reduction in design iterations. They perform fast analysis of large multi-million transistor designs and provide incremental what-if analysis capability.

Moscape will be premiering their technology and initial products at the 35th Design Automation Conference held June 15-19 in San Francisco, CA.

Moscape has a web site at www.moscape.com.

NOTE: Moscape is a trademark of Moscape, Inc.